FEATURE

The War on Soldering Defects under Area Array Packages: Head-in-Pillow and Non-Wet Open

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ALPHA

"If you know the enemy and know yourself, you need not fear the result of a hundred battles. If you know yourself but not the enemy, for every victory gained you will also suffer a defeat. If you know neither the enemy nor yourself, you will succumb in every battle."
—Sun Tzu, The Art of War

What is Head-in-Pillow and Non-Wet Open?

The most difficult aspect of any soldering defect on an area array package is the inability to observe the defect easily. It is important to understand the characteristics of soldering defects in order to identify the proper action to take to mitigate the defects in a soldering process.

Head-in-pillow (HiP) defects are soldering defects on area array packages characterized by a lack of coalescence between the solder paste deposit and the package solder bump. In these defects, the solder paste deposit coalesces properly with itself and typically wets to the PCB land. Displacement of each solder deposit (paste and bump) is a common feature of HiP defects.

Non-wet open (NWO) defects are soldering defects characterized by a lack of wetting to a PCB land by a fully coalesced solder deposit on an area array package. In this defect, the solder paste and the package solder bump coalesce together fully without wetting to the PCB land. A spherical or nearly spherical shape along the PCB side of the bump is a common feature of NWO defects.

What Head-in-Pillow and Non-Wet Open are not

It is important to discuss defects that can share some symptoms with HiP and NWO, in order to contrast against defects that require different mitigation actions. One example of a de-

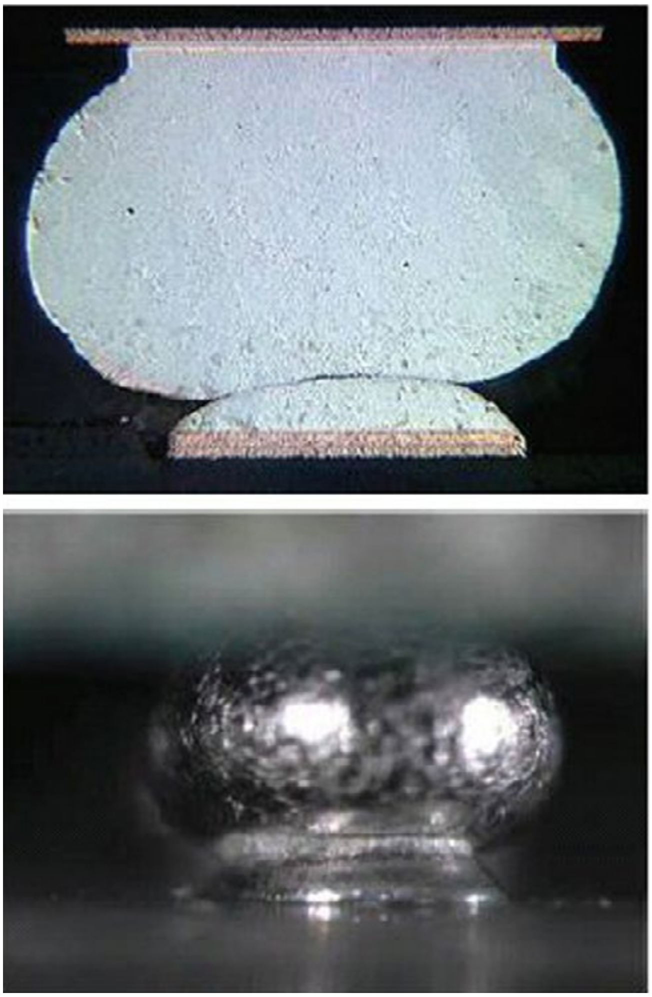

Figure 1: Head-in-pillow defect example, cross-section and endoscopic views.

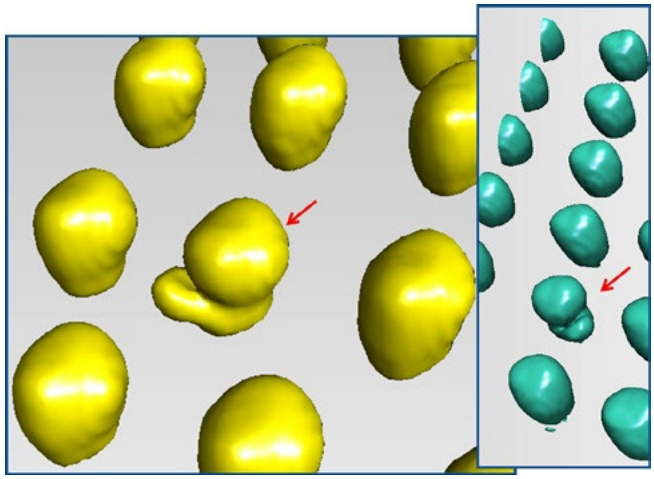

Figure 2: Head-in-pillow defect example, X-ray computer tomography view (courtesy Nordson Dage).

fect with similar symptoms to HiP and NWO is insufficient solder paste volume transfer during printing. In this case, it can appear that no wetting has occurred to the land and mimic NWO (especially if no paste has been transferred). If a small amount of paste has been printed, the resulting connection can initially appear to be consistent with HiP. Troubleshooting of HiP and NWO defects should include steps to ensure the solder paste printing process is properly controlled and performing well.

Another defect that can be confused with HiP is cold solder, which is characterized by a lack of coalescence of the solder paste deposit. HiP is a defect that occurs in the presence of a well-defined and controlled reflow process, which ensures coalescence of the solder paste deposit. Diagnosis of a defect as HiP should include an examination of the reflow profile to ensure that the process is not at risk of causing the occurrence of cold solder.

Non-wetting to a PCB land has many causes that should be familiar to most with experience troubleshooting solder defects. These defects can easily be confused with NWO since both defects share a symptom: poor wetting of a coalesced solder bump to the PCB land. The key difference is that NWO defects result in a solder bump that is spherical along the PCB side. A defect that is solely caused by poor PCB solderability will generally demonstrate the same shape as a typical area array solder connection: flatter and wider than a sphere and generally sharing the contour of the land along that interface. Testing the solderability of the PCB lands is an important step when attempting to determine if a wetting defect is a result of NWO defects.

Area Array Soldering and Defect Formation Mechanisms

During the soldering process, area array packages can appear to "drop" twice during a full reflow cycle. Each of the apparent drops by the package corresponds to an occurrence of coalescence of solder during the reflow process. The HiP and NWO defects represent the result of uncontrolled variation during one of those coalescence events.

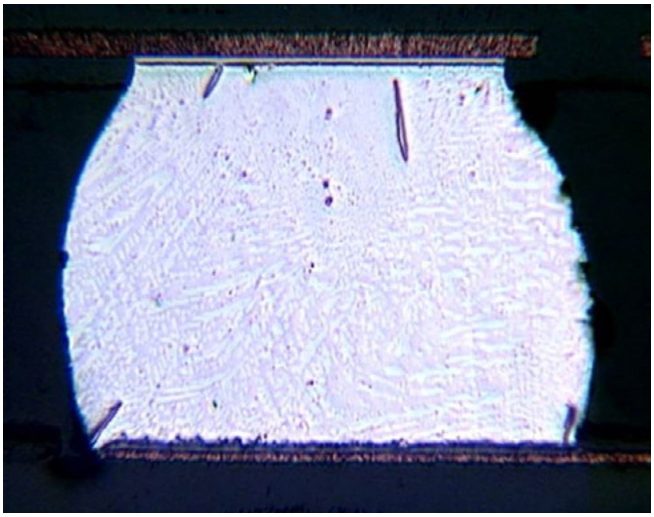

Figure 3: Typical area array solder connection cross-section.

As the PCBA reaches the liquidus temperatures of the solders, the solder paste will coalesce together into one large solder deposit. When this occurs, the package drops as the liquid solder is displaced by the mass of the package on the solder bumps. When the bumps and the paste have both reached a temperature where they are liquid, the separate solder volumes normally coalesce together and the package drops again. Upon cooling, the resulting solder connection has a characteristic shape with a flattened top and bottom (at package and PCB interfaces, respectively) and a rounded shape at the edges.

One mechanism of HiP formation is a failure of coalescence to occur between the solder paste and the solder bump. This prevents the joining of the solder volume into a single connection. Although the solder volumes share physical contact, they do not form a permanent connection and exhibit marginal electrical performance and no mechanical strength. Optimization of soldering process and materials can be effective at eliminating this type of HiP defect.

A second mechanism of HiP formation is also a primary driver of NWO defects. Both defects can be a result of warpage causing a co-planarity mismatch between the area array package and the PCB. This warpage can be described as having a "smile" or a "frown" warpage profile between the package and the PCB.

Figure 4: "Smile" and "frown" warpage profiles.

When a smile warpage occurs, the primary location for HiP and NWO defects to occur is closer to the edges of the package, where the package lifts away from the PCB. When a frown warpage occurs, the primary location for HiP and NWO defects is in the center of the package—again, where the package and the PCB have separated from each other during reflow. Mitigation of defects caused by warpage conditions is more difficult to troubleshoot and mitigate than pure coalescence failures.

HiP occurs when the two solder volumes reach liquidus when they are not in contact with each other due to the relative warpage mismatch of the assembly. Upon cooling, the dissimilar warpage of the assembly relaxes and the solder volumes come in to contact with each other for a short period before solidifying. This can allow for the molten solder bump and solder paste deposit to displace each other without coalescing together. Upon solidifying, the bumps form the namesake head (package bump) in pillow (solder paste deposit) feature as they rest against each other. This contact does not ensure a consistent

NWO defects also occur due to dissimilar warpage between the package and the PCB. This defect forms when the printed solder paste deposit has significantly more affinity for the solder bump than the PCB land prior to reflow. When the warpage mismatch separates the bump and land, the solder paste can remain in contact with the bump and reflow away from the PCB land surface. The solder paste and the package bump coalesce together, forming a larger bump at the package surface. The coalesced larger bump will form a spherical shape due to the surface tension of the molten solder. When the assembly cools, the dissimilar warpage relaxes and the bump typically comes to rest against the PCB land. The bump may form a small flat against the land or retain its spherical shape. This connection is not wetted to the

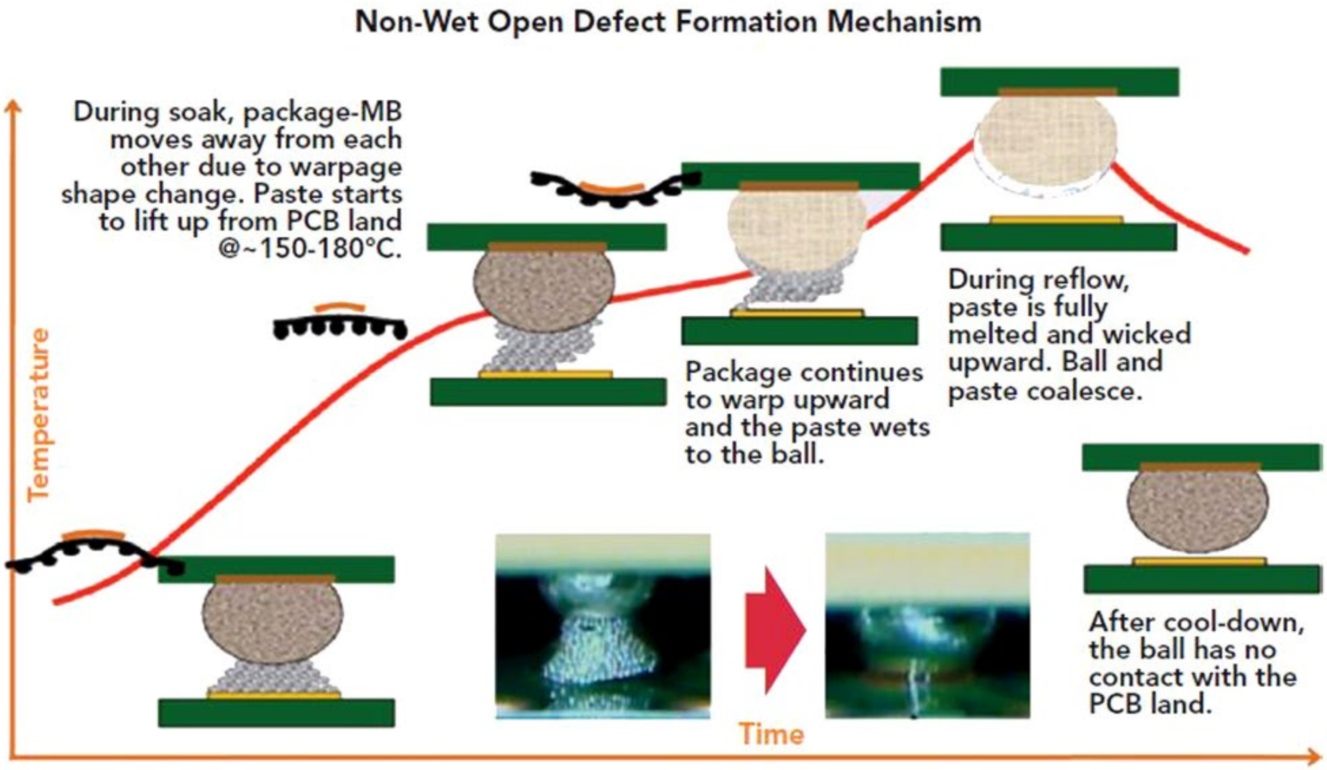

Figure 5: Non-wet open formation mechanism (courtesy Intel/SMTA)[1].

land and does not ensure a continuous, reliable electrical connection.

Strategies for Prevention of HiP: Process Factors

An improperly controlled process can be a significant contributor to HiP defects, particularly with the type that form due to an inability of the solder paste and solder bump to coalesce. The reflow profile, if defined in a way that exceeds the limits that a solder paste flux can withstand, can be a root cause of HiP. An extended preheat length or excessive soak temperature can exhaust the activator in a flux chemistry, thereby preventing the flux from performing its primary function: removing oxides from the surface of a solderable material (in this case, the solder bump). If the solder bump is oxidized, upon reaching liquidus temperatures it will not allow the molten solder deposit to coalesce across the oxide barrier.

The robustness of a solder paste to extended and hot preheat phase of a profile is specific to that formulation, but some general guidance is possible. Water-soluble pastes tend to be less robust to this condition than no-clean pastes, and water-soluble chemistries should be avoided if possible when HiP risk is a concern. Inert reflow can prevent this condition by preventing the solder bumps from oxidizing during preheat.

As the reflow profile is within the control of the assembler in most cases, it is important to experiment with the process to determine if HiP formation can be mitigated through reflow profile adjustments. It is important to understand that HiP can be low-occurrence defect, so testing should be performed on a sizeable sample of product in order to increase confidence that process performance has been improved. It is also important to understand that HiP can be caused by multiple factors, so process alterations can demonstrate improvement without complete elimination of the defect in some cases. Having a well-defined and robust reflow process is an important step to take first when troubleshooting HiP, as the other factors can be difficult to troubleshoot when process causes confound the solution by remaining an undiagnosed secondary cause of HiP.

Strategies for Prevention of HiP and NWO: Area Array Package Factors

Some area array packages are more prone to warpage than others, due to the materials and design used by package fabricators. Component warpage can be difficult to predict and measure, and the current industry standards on warpage control are insufficient to prevent HiP defects in many cases[2]. Discuss the methods used to measure characteristic warpage on an area array package. This measurement cannot be performed during an actual reflow process, so unprocessed parts must be tested and a statistical model of a component's typical warpage can be formed. In the six case studies presented by Chan et al., it was demonstrated that the characteristic warpage measured in cases where HiP was encountered did not exceed package warpage requirements from JEDEC and JEITA. In other words, a perfectly good (per industry standard requirements) area array package can be a risk factor for HiP and NWO!

This fact is important to understand when suddenly presented with HiP and/or NWO on a new assembly or new package when used in a process that has not historically experienced these types of defects. Most external observers are quick to blame the assembly process upon discovery of a new defect. When the characteristic warpage of a component exceeds the limits necessary to cause HiP/NWO, very little can be done from a reflow process modification standpoint to mitigate the defects. The physics involved are quite complicated and it is very difficult to predict how a change in a reflow profile will affect that warpage of a component. Most commonly, any steps that can be effective in reducing warpage are far outside the requirements to ensure a robust solder reflow process.

One strategy that can be effective in mitigating HiP and NWO caused by warpage is to modify the amount of solder paste printed to the affected locations. Tibbetts and Antinori discuss a mathematical model used to calculate the optimum solder paste deposit volume to combat a case of HiP on a package that has exhibited a tendency to warp during reflow[3]. The desired volume of solder varies across the package layout in response to the amount of warpage the package experiences during reflow. Their work demonstrates that there is a relationship between solder volume, component warpage, and tendency to form HiP defects. Since the assembler can control solder paste volume but not component warpage, the strategy presented by those authors is one that takes advantage of the factors that can be controlled in an attempt to mitigate the defects.

"The key properties of a solder paste that mitigate HiP and NWO defects are the paste's adhesion to the PCB land and package bump and the elasticity of the solder paste during reflow."

Strategies for Prevention of HiP and NWO: Solder Paste Materials

Some solder pastes are more robust to HiP and NWO formation than others. As discussed earlier as part of the process factors that can lead to HiP, water soluble formulations tend to be less robust to these defect conditions than their no-clean counterparts due to the no-clean pastes' inherently larger process window under reflow. However, within the family of no-clean solder pastes there can be a significant difference in performance with respect to HiP and NWO related to the physical properties of the pastes.

The key properties of a solder paste that mitigate HiP and NWO defects are the paste's adhesion to the PCB land and package bump and the elasticity of the solder paste during reflow. If a paste is able to stay in contact with both ends of the desired solder connection, the chances of forming a defect are greatly reduced.

A HiP defect that is caused by a separation of the paste from the bump during reflow can be prevented if that paste is tacky enough to stay in contact with the bump as warpage develops. The same goes for NWO defects caused by the paste pulling away from the PCB land; ensuring that the paste remains in contact with the land

and bump, even in the face of warpage, is critical to preventing the formation of that defect.

HiP-resistant pastes are also designed to have the ability to remain continuous as the paste is stretched during warpage under reflow. This is analogous to the elasticity of a rubber band when stretched. Ensuring the paste deposit remains continuous is critical to ensuring that the two solder volumes are able to coalesce once reflow has been achieved.

Unlike very familiar tests performed on solder paste materials (e.g., voiding resistance, slump resistance, and tack testing), there is no standard test for HiP and NWO resistance. Direct testing of physical properties (viscosity, tack, etc.) cannot be directly correlated to HiP and NWO performance. This leads to solder manufacturers creating their own proprietary test methods to characterize and benchmark paste performance with respect to these defects. There are some pitfalls to this type of testing and it is important to discuss with your solder paste manufacturer how the test data is generated and analyzed to ensure the data provides a good reflection of actual performance.

The major difficulty in developing HiP and NWO characterization tests is that these defects can occur with very low frequency, and it can be difficult to ensure formation of these defects in a repeatable fashion. Simply reflowing a test vehicle with a variety of area array packages is not sufficient to demonstrate robustness to HiP and NWO. Test of this nature, which are likely to result in zero HiP or NWO defects under typical conditions, fall prey to a data fallacy: If a test sample with no defects is a common outcome of a test, how can two test samples be compared against each other when they both result in zero defects? Is sample A better, worse, or the same as sample B, as both have zero defects? In addition, can either sample A or sample B be advertised as being completely resistant to the defect? In this situation, samples A and B cannot be differentiated from each other and there is no guarantee that either formula has solved the problem.

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One hallmark of a good characterization test is create a test that is “designed to fail” by creating conditions that are at the very limits of performance expectations. In other words, designing a test where defects are assured to occur then changing inputs and measuring the rate at which defects occur allows for relative comparison of each sample. These types of tests are excellent at identifying when performance has been improved or deprecated when comparing multiple test samples.

Another consideration when analyzing test data is to be skeptical of claims to “eliminate HiP defects” by citing test data. Characterization tests are excellent tests when used as a tool to compare performance across similar conditions. Using a characterization test to make a claim of complete elimination of a defect is an example where a high risk of an error of the first kind (a false positive) exists. The old adage that you cannot prove a negative holds here. A claim that a solder paste eliminates HiP and NWO defects is a strong claim, but basing that claim on testing performed under controlled conditions only proves the claim until the first example from the field where HiP or NWO is discovered. A claim that a particular solder paste is more resistant to or less likely to experience HiP/NWO defects than other solder pastes is a more appropriate claim to make based on characterization testing.

A third consideration when analyzing a solder paste manufacturer’s HiP and NWO test data is sample size. All statistics are estimates to some degree, and those estimates gain precision with increased samples. Characterization testing for HiP and NWO should be performed in relatively large sample sizes in order to increase confidence that the results will hold true when applied to a large-scale manufacturing process.

Final Thoughts

HiP and NWO defects are particularly difficult to troubleshoot and mitigate. As Sun Tzu points outs, if the reflow process is not well defined and controlled (you do not know yourself) you will succumb in every battle against HiP and NWO. Having a well-controlled reflow process but not understanding the intricacies of HiP and NWO (you know yourself but not your enemy) only ensures that you will be unable to fully defeat HiP and NWO, and should expect to suffer mix of defeat and victory. Fully understanding the mechanism behind HiP and NWO formation (knowing your enemy and yourself) means you do not need to fear the result of assembling a hundred boards. Who knew that Sun Tzu would make a good soldering engineer? **SMT**

References

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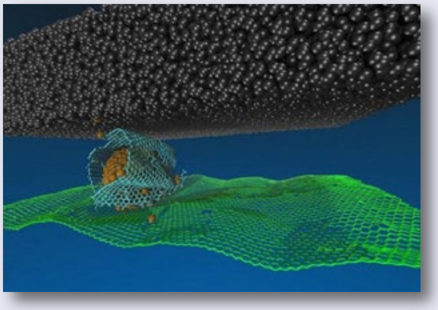
Simulations Lead to Design of Near-frictionless Material

Argonne scientists have developed a hybrid material that exhibited superlubricity at the macroscale for the first time. ALCF researchers helped enable the groundbreaking simulations by overcoming a performance bottleneck that doubled the speed of the team's code.

While reviewing the simulation results of a promising new lubricant material, Argonne researcher Sanket Deshmukh stumbled upon a new phenomenon.

"Sanket said, 'you have got to come over here and see this. I want to show you something really cool,'" said Subramanian Sankaranarayanan, Argonne computational nanoscientist, who led the simulation work at the Argonne Leadership Computing Facility (ALCF), a DOE Office of Science User Facility.



They were amazed by what the computer simulations revealed. When the lubricant materials—graphene and diamond-like carbon (DLC)—slid against each other, the graphene began rolling up to form hollow cylindrical "scrolls" that helped to practically eliminate friction. These so-called nanoscrolls represented a completely new mechanism for superlubricity, a state in which friction essentially disappears.

"The nanoscrolls combat friction in very much the same way that ball bearings do by creating separation between surfaces," said Deshmukh, who finished his postdoctoral appointment at Argonne in January.

Superlubricity is a highly desirable property. Considering that nearly one-third of every fuel tank is spent overcoming friction in automobiles, a material that can achieve superlubricity would greatly benefit industry and consumers alike. Such materials could also help increase the lifetime of countless mechanical components that wear down due to incessant friction.